Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claim 1-5, 7, 9, 11, 14-18, 20, 22, 24, 26-30, 32, 34, 36, 40-45, 47 and 49 as follows:

Listing of Claims:

1. (Currently amended) A memory module, comprising:

a plurality of memory devices; and

a memory hub, comprising:

a link interface receiving memory requests for access to at least one of the memory devices;

a memory device interface coupled to the memory devices, the memory device interface being operable to transmit~~couple~~ memory requests to the memory devices for access to at least one of the memory devices and to receive read data responsive to at least some of the memory requests;

a posted write buffer coupled to the link interface and the memory device interface, the posted write buffer being operable to store write memory requests and to subsequently transmit~~couple~~ the write memory requests to the memory device interface; and

a read request path operable to transmit~~couple~~ read memory requests from the link interface to the memory device interface and to transmit~~couple~~ read data from the memory device interface to the link interface.

2. (Currently amended) The memory module of claim 1 wherein the read request path comprises a memory sequencer coupled to the link interface and the memory device interface, the memory sequencer being operable to transmit~~couple~~ memory requests to the memory device interface responsive to memory requests received from the link interface.

3. (Currently amended) The memory module of claim 2 wherein the posted write buffer comprises coherency circuitry that is operable to receive read memory requests from the link interface and is operable to determine if read data called for by the read request is stored in the posted write buffer and to generate a hit signal responsive thereto, and wherein the memory sequencer is coupled to receive the hit signal from the posted write buffer and is operable to transmit~~couple~~ memory requests to the memory device interface responsive to memory requests received from the link interface only in the absence of the hit signal.

4. (Currently amended) The memory module of claim 1 wherein the posted write buffer is operable to transmit~~couple~~ the write memory requests to the memory device interface only when neither the memory hub nor the memory devices are busy servicing read memory requests .

5. (Currently amended) The memory module of claim 1 wherein the posted write buffer further comprises coherency circuitry coupled to receive read memory requests from the link interface, the coherency circuitry being operable to determine from each read memory request whether the read memory request is directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface, the coherency circuitry being operable to transmit~~couple~~ the read data responsive to the read memory request from the posted write buffer to the link interface in the event the read memory request is directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface.

6. (Original) The memory module of claim 1 wherein the memory hub further comprises a multiplexer having a first input port coupled to receive read data from the posted write buffer, a second input port coupled to receive read data from the memory device interface and an output port coupled to the link interface to apply read data to the link interface, the multiplexer further having a control terminal coupled to the posted write buffer, the posted

write buffer generating a control signal to cause the multiplexer to couple the output port to the first input port in the event the read memory request is directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface, and to generate a control signal to cause the multiplexer to couple the output port to the second input port in the event the read memory request is not directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface.

7. (Currently amended) The memory module of claim 1 wherein the posted write buffer is operable to store posted write memory requests until the number of posted write memory requests accumulated exceeds a predetermined number, and to thereafter transmit~~couple~~ the posted write memory requests to the memory device interface.

8. (Original) The memory module of claim 7 wherein the posted write buffer is operable to vary the predetermined number as a function of an operating parameter of the memory module.

9. (Currently amended) The memory module of claim 1 wherein the posted write buffer is operable to store posted write memory requests until the posted write memory requests have been stored for more than a predetermined duration, and to thereafter transmit~~couple~~ the posted write memory requests to the memory device interface.

10. (Original) The memory module of claim 9 wherein the posted write buffer is operable to vary the predetermined duration as a function of an operating parameter of the memory module.

11. (Currently amended) The memory module of claim 1 wherein the posted write buffer is operable to store posted write memory requests as long as the number of posted write memory requests accumulated does not exceed a predetermined number and the posted

write memory requests have not been stored for more than a predetermined duration, and to transmit~~couple~~ the posted write memory requests to the memory device interface if either the number of posted write memory requests accumulated exceeds the predetermined number or the posted write memory requests have been stored for more than the predetermined duration.

12. (Original) The memory module of claim 1 wherein the link interface comprises an optical input/output port.

13. (Original) The memory module of claim 1 wherein the memory devices comprise dynamic random access memory devices.

14. (Currently amended) A memory hub, comprising:

a link interface receiving memory requests from a memory controller;

a memory device interface operable to output memory requests and to receive read data responsive to the memory requests output by the memory device interface;

a posted write buffer coupled to the link interface and the memory device interface, the posted write buffer being operable to store write memory requests and to subsequently transmit~~couple~~ the write memory requests to the memory device interface; and

a read request path operable to transmit~~couple~~ read memory requests from the link interface to the memory device interface and to transmit~~couple~~ read data from the memory device interface to the link interface.

15. (Currently amended) The memory hub of claim 14 wherein the read request path comprises a memory sequencer coupled to the link interface and the memory device interface, the memory sequencer being operable to transmit~~couple~~ memory requests to the memory device interface responsive to memory requests received from the link interface.

16. (Currently amended) The memory hub of claim 15 wherein the posted write buffer comprises coherency circuitry that is operable to receive read memory requests from

the link interface and is operable to determine if read data called for by the read request is stored in the posted write buffer and to generate a hit signal responsive thereto, and wherein the memory sequencer is coupled to receive the hit signal from the posted write buffer and is operable to transmit~~couple~~ memory requests to the memory device interface responsive to memory requests received from the link interface only in the absence of the hit signal.

17. (Currently amended) The memory hub of claim 14 wherein the posted write buffer is operable to transmit~~couple~~ the write memory requests to the memory device interface only when neither the memory hub nor the memory devices are busy servicing read memory requests .

18. (Currently amended) The memory hub of claim 14 wherein the posted write buffer further comprises coherency circuitry coupled to receive read memory requests from the link interface, the coherency circuitry being operable to determine from each read memory request whether the read memory request is directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface, the coherency circuitry being operable to transmit~~couple~~ the read data responsive to the read memory request from the posted write buffer to the link interface in the event the read memory request is directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface.

19. (Original) The memory hub of claim 14 wherein the memory hub further comprises a multiplexer having a first input port coupled to receive read data from the posted write buffer, a second input port coupled to receive read data from the memory device interface and an output port coupled to the link interface to apply read data to the link interface, the multiplexer further having a control terminal coupled to the posted write buffer, the posted write buffer generating a control signal to cause the multiplexer to couple the output port to the first input port in the event the read memory request is directed to a memory address to which a

write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface, and to generate a control signal to cause the multiplexer to couple the output port to the second input port in the event the read memory request is not directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface.

20. (Currently amended) The memory hub of claim 14 wherein the posted write buffer is operable to store posted write memory requests until the number of posted write memory requests accumulated exceeds a predetermined number, and to thereafter transmit~~couple~~ the posted write memory requests to the memory device interface.

21. (Original) The memory module of claim 20 wherein the posted write buffer is operable to vary the predetermined number as a function of an operating parameter of the memory hub.

22. (Currently amended) The memory hub of claim 14 wherein the posted write buffer is operable to store posted write memory requests until the posted write memory requests have been stored for more than a predetermined duration, and to thereafter transmit~~couple~~ the posted write memory requests to the memory device interface.

23. (Original) The memory hub of claim 22 wherein the posted write buffer is operable to vary the predetermined duration as a function of an operating parameter of the memory module.

24. (Currently amended) The memory hub of claim 14 wherein the posted write buffer is operable to store posted write memory requests as long as the number of posted write memory requests accumulated does not exceeds a predetermined number and the posted write memory requests have not been stored for more than a predetermined duration, and to transmit~~couple~~ the posted write memory requests to the memory device interface if either the

number of posted write memory requests accumulated exceeds the predetermined number or the posted write memory requests have been stored for more than the predetermined duration.

25. (Original) The memory hub of claim 14 wherein the link interface comprises an optical input/output port.

26. (Currently amended) A computer system, comprising:

a central processing unit ("CPU");

a system controller coupled to the CPU, the system controller having an input port and an output port;

an input device coupled to the CPU through the system controller;

an output device coupled to the CPU through the system controller;

a storage device coupled to the CPU through the system controller;

a plurality of memory modules, each of the memory modules comprising:

a plurality of memory devices; and

a memory hub, comprising:

a link interface receiving memory requests for access to at least one of the memory devices;

a memory device interface coupled to the memory devices, the memory device interface being operable to transmit~~couple~~ memory requests to the memory devices for access to at least one of the memory devices and to receive read data responsive to at least some of the memory requests;

a posted write buffer coupled to the link interface and the memory device interface, the posted write buffer being operable to store write memory requests and to subsequently transmit~~couple~~ the write memory requests to the memory device interface; and

a read request path operable to transmit~~couple~~ read memory requests from the link interface to the memory device interface and to

transmit~~couple~~ read data from the memory device interface to the link interface; and

a communications link coupled between the system controller and each of the memory modules for transmitting~~coupling~~ memory requests and read data between the system controller and the memory modules in the respective memory modules.

27. (Currently amended) The computer system of claim 26 wherein the read request path comprises a memory sequencer coupled to the link interface and the memory device interface, the memory sequencer being operable to transmit~~couple~~ memory requests to the memory device interface responsive to memory requests received from the link interface.

28. (Currently amended) The computer system of claim 27 wherein the posted write buffer comprises coherency circuitry that is operable to receive read memory requests from the link interface and is operable to determine if read data called for by the read request is stored in the posted write buffer and to generate a hit signal responsive thereto, and wherein the memory sequencer is coupled to receive the hit signal from the posted write buffer and is operable to transmit~~couple~~ memory requests to the memory device interface responsive to memory requests received from the link interface only in the absence of the hit signal.

29. (Currently amended) The computer system of claim 26 wherein the posted write buffer is operable to transmit~~couple~~ the write memory requests to the memory device interface only when neither the memory hub nor the memory devices are busy servicing read memory requests .

30. (Currently amended) The computer system of claim 26 wherein the posted write buffer further comprises coherency circuitry coupled to receive read memory requests from the link interface, the coherency circuitry being operable to determine from each read memory request whether the read memory request is directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled

to the memory device interface, the coherency circuitry being operable to transmit~~couple~~ the read data responsive to the read memory request from the posted write buffer to the link interface in the event the read memory request is directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface.

31. (Original) The computer system of claim 26 wherein the memory hub further comprises a multiplexer having a first input port coupled to receive read data from the posted write buffer, a second input port coupled to receive read data from the memory device interface and an output port coupled to the link interface to apply read data to the link interface, the multiplexer further having a control terminal coupled to the posted write buffer, the posted write buffer generating a control signal to cause the multiplexer to couple the output port to the first input port in the event the read memory request is directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface, and to generate a control signal to cause the multiplexer to couple the output port to the second input port in the event the read memory request is not directed to a memory address to which a write memory request has been stored in the posted write buffer and has not yet been coupled to the memory device interface.

32. (Currently amended) The computer system of claim 26 wherein the posted write buffer is operable to store posted write memory requests until the number of posted write memory requests accumulated exceeds a predetermined number, and to thereafter transmit~~couple~~ the posted write memory requests to the memory device interface.

33. (Original) The computer system of claim 32 wherein the posted write buffer is operable to vary the predetermined number as a function of an operating parameter of the computer system.

34. (Currently amended) The computer system of claim 26 wherein the posted write buffer is operable to store posted write memory requests until the posted write memory requests have been stored for more than a predetermined duration, and to thereafter transmit~~couple~~ the posted write memory requests to the memory device interface.

35. (Original) The computer system of claim 34 wherein the posted write buffer is operable to vary the predetermined duration as a function of an operating parameter of the computer system.

36. (Currently amended) The computer system of claim 26 wherein the posted write buffer is operable to store posted write memory requests as long as the number of posted write memory requests accumulated does not exceeds a predetermined number and the posted write memory requests have not been stored for more than a predetermined duration, and to transmit~~couple~~ the posted write memory requests to the memory device interface if either the number of posted write memory requests accumulated exceeds the predetermined number or the posted write memory requests have been stored for more than the predetermined duration.

37. (Original) The computer system of claim 26 wherein the link interface comprises an optical input/output port.

38. (Original) The computer system of claim 26 wherein the memory devices comprise dynamic random access memory devices.

39. (Original) The computer system of claim 26 wherein the communications link comprises an optical communications link.

40. (Currently amended) In a computer system, a method of reading data from a plurality of memory modules, comprising:

receiving memory requests at each of the plurality of memory modules, the memory requests requesting access to a memory device in the memory module, the memory requests including read requests and write requests;

transmitting~~coupling~~ at least some of the read memory requests to the memory device in the memory module receiving the read request;

transmitting~~coupling~~ read data from the memory module responsive to the read memory request;

accumulating the write requests in the memory module without immediately transmitting~~coupling~~ the write requests to the memory devices in the memory module receiving the write request; and

subsequently transmitting~~coupling~~ each of the accumulated write requests to the memory device in the memory module receiving the write request.

41. (Currently amended) The method of claim 40, further comprising:

determining in each memory module receiving a read request if the read request is directed to a memory address for which an accumulated write request is directed but not yet coupled to the memory device;

if the read request is directed to a memory address for which an accumulated write request is directed but not yet coupled to the memory device, transmitting~~coupling~~ the read data from the accumulated write requests; and

if the read request is not directed to a memory address for which an accumulated write request is directed but not yet coupled to the memory device, transmitting~~coupling~~ the read data from the memory device.

42. (Currently amended) The method of claim 40, further comprising:

determining in each memory module receiving a read request if the read request is directed to a memory address for which an accumulated write request is directed but not yet coupled to the memory device; and

if the read request is not directed to a memory address for which an accumulated write request is directed but not yet coupled to the memory device, transmitting~~coupling~~ the read request to the memory device in the memory module receiving the read request.

43. (Currently amended) The method of claim 40 wherein the act of subsequently transmitting~~coupling~~ each of the accumulated write requests to the memory device in the memory module receiving the write request comprises subsequently transmitting~~coupling~~ each of the accumulated write requests to the memory device in the memory module receiving the write request only when the memory device is not busy servicing a read request.

44. (Currently amended) The method of claim 40, further comprising:

determining from each read memory request whether the read memory request is directed to a memory address to which a write memory request has been accumulated but not yet coupled to the memory device;

transmitting~~coupling~~ the read data responsive to the read memory request from the accumulated write requests in the event the read memory request is directed to a memory address to which a write memory request has been accumulated but not yet coupled to the memory device.

45. (Currently amended) The method of claim 40 wherein the act of subsequently transmitting~~coupling~~ each of the accumulated write requests to the memory device in the memory module receiving the write request comprises:

accumulating write requests until the number of write requests accumulated exceeds a predetermined number; and

when the number of write requests accumulated exceeds the predetermined number, transmitting~~coupling~~ the write requests to the memory device.

46. (Original) The method of claim 45, further comprising varying the predetermined number as a function of an operating parameter of the computer system.

47. (Currently amended) The method of claim 40 wherein the act of subsequently transmitting~~coupling~~ each of the accumulated write requests to the memory device in the memory module receiving the write request comprises:

accumulating write requests until the write requests have been accumulated for more than a predetermined duration;

when each of the write requests has been accumulated for more than the predetermined duration, transmitting~~coupling~~ the write request to the memory device.

48. (Original) The method of claim 47, further comprising varying the predetermined duration as a function of an operating parameter of the computer system.

49. (Currently amended) The method of claim 40 wherein the act of subsequently transmitting~~coupling~~ each of the accumulated write requests to the memory device in the memory module receiving the write request comprises:

accumulating write requests until the number of write requests accumulated exceeds a predetermined number or the write requests have been accumulated for more than a predetermined duration; and

when the number of write requests accumulated exceeds the predetermined number or when a write request has been accumulated for more than the predetermined duration, transmitting~~coupling~~ the write request to the memory device.

50. (Original) The method of claim 40 wherein the memory devices comprise dynamic random access memory devices.